IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Day et al.	§	Confirmation No.: 5112
	§	
Serial Number: 10/606,582	§	
	§	Group Art Unit: 2181
Filed: June 26, 2003	§	
	§	
For: SYSTEM AND METHOD FOR TRACKING MESSAGES BETWEEN A PROCESSING UNIT AND AN EXTERNAL DEVICE	§	Examiner: Ernest Unelus
	§	

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICANTS' REPLY BRIEF

Applicant-inventors ("Applicants") and assignee International Business Machines Corporation respectfully submit the present brief in support of the patentability of the claims of the above-referenced application.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, of Armonk, New York, assignee of the interests in the invention from the named inventors.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 20-35 are pending. Of these, Claims 20 and 28 are independent Claims. Applicant has cancelled Claims 7-13 and 15-18. Applicant has withdrawn Claims 1-6, 14, and 19. The Examiner has withdrawn the objections to the drawings under 37 CFR 1.83(a) and the rejections of Claims 28-35 under 35 U.S.C. §101 and of Claims 20-35 under 35 U.S.C. §112, first paragraph.

Applicants appeal the Examiner's rejections of Claims 20-35 under 35 U.S.C. §103(a).

IV. STATUS OF AMENDMENTS

The Claims stand as amended in the Response to an Office Action dated April 23, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

As recited in Applicants' Appeal Brief.

VI. GROUNDS OF REJECTION TO BE REVIEWED

Whether Claims 20-35 are patentable over Young (US 6,408,354) in view of Stuber et al. (US 6,801,972) under 35 U.S.C. §103(a).

VII. ARGUMENT IN REPLY

A. Grouping of Claims

Claims 20 and 28 are independent. For purposes of this appeal, Applicants consider each of the independent Claims, and their respective dependent Claims, as separate groups. Thus, the groups of Claims are 20-27 and 28-35.

B. Summary of Pertinent Prosecution

As recited in Applicants' Appeal Brief.

C. The Examiner's Rejections Were Procedurally and Factually in Error

The Examiner's answer further supports Applicants' assertion that the Examiner's rejections were procedurally and factually in error.

Regarding Claims 20 and 28 (the independent Claims from which all of the Pending Dependent Claims depend), the Examiner stated that Young discloses:

"an external device (ED) (SCSI module 230 of fig.3. . .)"; Final Action, Page 5;

". . . a write register (bi-directional data buffer 345 of fig. 3)"; Final Action, Page 6; and

"incrementing a write channel count upon receipt of outbound data from the PU by the ED (see col. 7, lines 62-63, which discloses, 'A second counter is incremented as each unit of data is transferred to bi-directional buffer 345')"; Final Action, Page 6.

Applicants respectfully submit that the Examiner's proposed combination, even as described by the Examiner in the Examiner's Answer, fails to teach "incrementing a write channel count upon receipt of outbound data from the PU by the ED," as recited in the claims. Specifically, the Examiner emphasizes that Young purportedly teaches "incrementing by the ED" instead of incrementing the write channel count "upon receipt of outbound data . . . by the ED" as recited in the Claims.

In the Examiner's Answer, the Examiner characterizes Young's SCSI Module 230 as corresponding to the Pending Claim's ED, which communicates with "a bi-directional data

channel 303 functioning as a processing unit." Examiner's Answer, Page 8. The Examiner also states that, in Young, "the buffer count increases when data is transferring into the buffer [354 of channel 303]." Examiner's Answer, Page 9. To use the Claim language, according to the Examiner, Young teaches incrementing a write channel count upon receipt of outbound data from the PU *by the PU's outbound data buffer*. The Examiner's own characterization of Young therefore directly contradicts the language of the Claims.

Put plainly, according to the Examiner, the claims recite incrementing the write channel count when the ED receives the outbound data and Young teaches incrementing the write channel count when the PU's outbound buffer receives the outbound data. Yet the Examiner insists these are equivalent: "Examiner maintains that Young's teachings of incrementing the write channel by the write register is equivalent to applicant's claim language regarding incrementing by the ED, since Young's write register is inside of Young's PU." Examiner's Answer, Page 9 (emphasis omitted). Applicants respectfully submit that this is clearly a misapplication of Young.

Finally, the Examiner's revisions of Applicants' argument completely mischaracterize the substance of Applicants' argument. The Examiner states:

> Further, applicant argues "Young teach incrementing the write channel . . . by the **write register** . . . however, the unique invention embodied therein recites 'incrementing a write channel . . . **by the ED** . . . therefore cannot support a rejection under Section 103 . . ."
>
> Examiner's Answer, Page 9 (underline omitted). What Applicants actually argued was:
>
> Young teaches **incrementing the write channel count upon receipt of outbound data from the PU by the write register**. As recited in the Claims, however, the unique invention embodied therein recites "incrementing a write channel count upon receipt of outbound data from the PU by the ED." Claims 20, 28. As such, the Examiner's offered *prima facie* case is insufficient on its face and therefore cannot support a rejection under Section 103.

Applicants' Appeal Brief, Page 12 (emphasis added). As described above, the Examiner's own characterization of Young directly contradicts the Claim language. As such, Applicants respectfully submit that The Examiner's offered *prima facie* case remains insufficient on its face, and therefore cannot support a rejection under Section 103.

Accordingly, Applicants respectfully submit that the Examiner's stated grounds are insufficient to maintain the Final Rejection. Applicants therefore respectfully request that the Final Rejections be withdrawn and that Claims 20-35 be allowed.

VIII. CLAIMS APPENDIX

See Attached.

IX. EVIDENCE APPENDIX

NONE.

X. RELATED PROCCEDINGS APPENDIX

NONE.

XI. CONCLUSION

For the foregoing reasons, it is respectfully submitted that the Final Rejections of Claims 20-35 under 35 U.S.C. §112, first paragraph, and §103(a) and of Claims 28-35 under 35 U.S.C. §101 are improper and should be reversed. Applicants respectfully request that the rejections of Claims 20-35 be withdrawn and that Claims 20-35 be allowed.

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Applicants hereby authorize the Director to charge the required fee for the filing of this Reply Brief to Deposit Account No. 09-0447 of IBM Corporation. Applicants do not believe that any other fees are due; however, in the event that any other fees are due, the Director is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 09-0447 of IBM Corporation.

Respectfully submitted,

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Dated: June 30, 2008

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VIII – APPENDIX – CLAIMS ON APPEAL

1. (Withdrawn) A system for use by a PU (processing unit) in communicating externally in a symmetrical multiprocessor system, comprising:

PU issue and control logic means;

PU data flow means interconnected to the PU issue and control logic means;

PU channel logic means interconnected to the PU issue and control logic means and the PU data flow means, wherein said PU channel logic means includes:

channel read data means and channel write data means interconnected between the PU data flow means and the PU channel logic means;

channel and data input and output port means interconnected to the PU channel logic means;

channel stall signal output means interconnected from the PU channel logic means to the PU issue command control logic means; and

channel instruction means interconnecting the PU issue and control logic means to the PU channel logic means.

2. (Withdrawn) The apparatus of claim 1, comprising in addition:

means for keeping track of the number of communications pending with said specified device; and

means for modifying further PU actions when the number of communications with said specified device reaches a given predetermined number.

3. (Withdrawn) The apparatus of claim 2 wherein the means for modifying PU action operates to prevent further communication with said specified device until the number of communications with said specified device is caused to be altered.

4. (Withdrawn) The apparatus of claim 1, comprising in addition:

means for assigning a channel for communications with a given external device;

means for placing communications for said given external device in a given storage means;

means for tracking the number of communications, for a given one of read or write instructions, from a PU to a given external device in a given counter associated with said channel that has been assigned;

means for tracking the number of communications, for said given one of read or write instructions, to the PU from the given external device to alter the count in the counter in a direction opposite from the counter movement when said instructions are sent from the PU; and

means for validating data in said given storage means when the count for said channel is at a given value.

5. (Withdrawn) The apparatus of claim 1, comprising in addition:

means for maintaining a count of register inputs versus outputs; and

means for retrieving data as valid when the count is other than a given predetermined value.

6. (Withdrawn) The apparatus of claim 1, comprising in addition:

means for maintaining a count of register inputs versus outputs; and

means for preventing further writing of data into said register when the count reaches a given predetermined value.

7. – 13. (Cancelled)

14. (Withdrawn) A microprocessor, comprising:

read channels;

write channels;

incoming data counting mechanisms for at least some of said read and write channels; and

instruction processing means responding to external device generated instructions requesting a determination of the count in said data counting mechanism of at least one of said write channel and read channels having counting mechanisms.

15. – 18. (Cancelled)

19. (Withdrawn) Apparatus for transmitting data between a PU and an external device, comprising:

a data storage register;

means, comprising a part of said register, operable to accumulate data received from multiple writes directed to said register; and

means, comprising a part of said register, operable to transmit all data accumulated in said register in response to a single received read instruction.

20. (Previously Presented) A method for tracking communications between a processing unit (PU) and an external device (ED), comprising:

receiving, by the PU, data from the ED, into a read register;

sending, by the PU, data to the ED, from a write register;

incrementing a read channel count upon receipt of inbound data from the ED by the PU;

issuing a read channel instruction to decrement the read channel count upon processing of received inbound data by the PU;

incrementing a write channel count upon receipt of outbound data from the PU by the ED;

issuing a write channel instruction to decrement the write channel count upon transmission by the PU of the outbound data to the ED;

accessing the read channel count; and

comparing the accessed read channel count with a predetermined range to determine whether the PU has received data from the ED.

21. (Previously Presented) The method as recited in Claim 20, further comprising associating an active channel with the read register and the write register.

22. (Previously Presented) The method as recited in Claim 21, wherein issuing a write channel instruction further comprises writing data externally to the PU.

23. (Previously Presented) The method as recited in Claim 21, wherein issuing a write channel instruction further comprises writing data to an internal register of the PU.

24. (Previously Presented) The method as recited in Claim 21, wherein issuing a read channel instruction further comprises returning read data to a PU dataflow.

25. (Previously Presented) The method as recited in Claim 20, further comprising associating a passive channel with the read register and the write register.

26. (Previously Presented) The method as recited in Claim 25, wherein issuing a write channel instruction further comprises storing write data locally for an external read operation.

27. (Previously Presented) The method as recited in Claim 25, wherein issuing a read channel instruction further comprises returning read data to a PU dataflow.

28. (Previously Presented) A computer program product for tracking communications between a processing unit (PU) and an external device (ED), the computer program product having a computer-readable medium with a computer program embodied thereon, the computer program comprising:

computer code for receiving, by the PU, data from the ED, into a read register;

computer code for sending, by the PU, data to the ED, from a write register;

computer code for incrementing a read channel count upon receipt of inbound data from the ED by the PU;

computer code for issuing a read channel instruction to decrement the read channel count upon processing of received inbound data by the PU;

computer code for incrementing a write channel count upon receipt of outbound data from the PU by the ED;

computer code for issuing a write channel instruction to decrement the write channel count upon transmission by the PU of the outbound data to the ED; and

computer code for accessing the read channel count; and

computer code for comparing the accessed read channel count with a predetermined range to determine whether the PU has received data from the ED.

29. (Previously Presented) The computer program product as recited in Claim 28, further comprising computer code for associating an active channel with the read register and the write register.

30. (Previously Presented) The computer program product as recited in Claim 29, wherein issuing a write channel instruction further comprises writing data externally to the PU.

31. (Previously Presented) The computer program product as recited in Claim 29, wherein issuing a write channel instruction further comprises writing data to an internal register of the PU.

32. (Previously Presented) The computer program product as recited in Claim 29, wherein issuing a read channel instruction further comprises returning read data to a PU dataflow.

33. (Previously Presented) The computer program product as recited in Claim 28, further comprising computer code for associating a passive channel with the read register and the write register.

34. (Previously Presented) The computer program product as recited in Claim 33, wherein issuing a write channel instruction further comprises storing write data locally for an external read operation.

35. (Previously Presented) The method as recited in Claim 33, wherein issuing a read channel instruction further comprises returning read data to a PU dataflow.